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MEMS' Olympic moment 22

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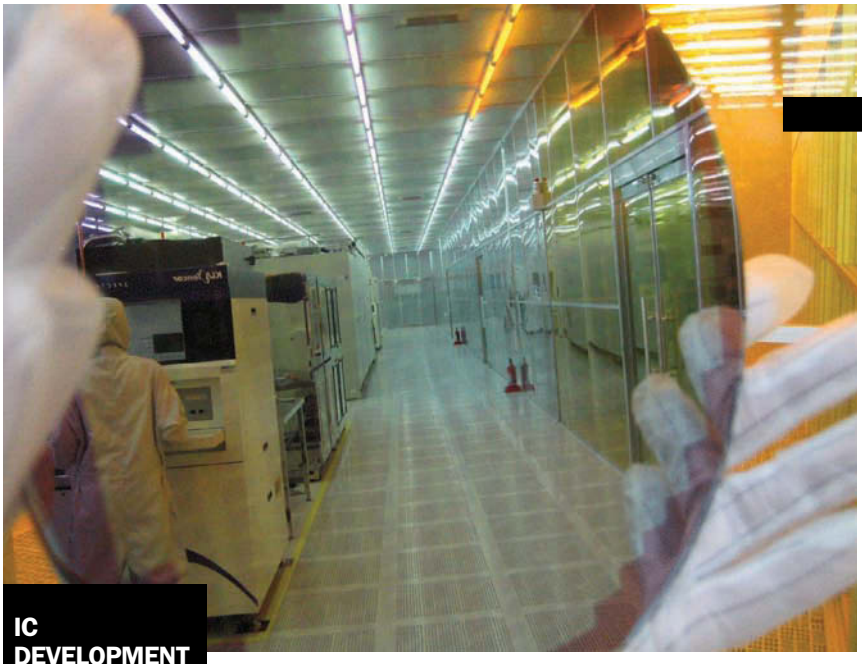

BeSang 3-D wafer reflecting image of the clean room in which it was processed

IC DEVELOPMENT

BeSang debuts first 3-D chip

By R. Colin Johnson

THE WORLD'S FIRST 3-D chip process is ready for licensing from the fabless semiconductor design house BeSang Inc.

BeSang fabricated demonstration chips with 128 million vertical transistors for memory bit cells above the control logic. The chips were designed at the National Nanofab Center (Daejeon, South Korea) and Stanford Nanofab (Palo Alto, Calif.). BeSang said its process, which is protected by more than 25 patent applications, will allow flash, DRAM and SRAM to be placed atop logic, microprocessor cores and systems on chip (SoCs).

BeSang claims it achieved 3-D by fabricating logic circuitry using a high-temperature process on the bottom and by fabricating memory circuitry using a low-temperature process on top of the logic. By placing logic and memory on different layers of the same 3-D chip, BeSang's process packs in more die per wafer, which translates into lower costs per die.

"BeSang was founded five years ago to work on 3-D IC technology [and] has introduced a single-chip 3-D IC process that is ready for commercialization," said Sang-Yun Lee, founder and CEO of the Beaverton, Ore., company.

At BeSang ("flying high" in Korean) Lee perfected the first true 3-D IC process with former Samsung engineer Junil Park, developer of the first atomic layer deposition tool for high-k dielectrics. Because the new IC processing technique does not stack dies, the company claims normal cooling techniques will work because its slightly thicker 3-D chips generate no additional heat.

A new logic arrangement

Current planar (2-D) chips that contain memory must surround their memory arrays with logic circuitry to address bits and to perform logic functions. Placing memory and logic alongside each other forces the use of long interconnection lines between the two.

BeSang, on the other hand, placed logic circuitry on the bottom layer and the memory bit cells on the higher layers of the 3-D chip, enabling very compact designs with very short interconnection lines between them.

"Systems-on-chip puts logic alongside memory on the same chip, but have had to compromise on performance since both were fabricated with the same process," said Simon Sze, who co-invented the floating-gate transistor for nonvolatile memory cells in 1967 at Bell Labs. Sze is now a professor at the National Chiao Tung University in Taiwan.

"By putting the memory devices on top of the logic devices, using separately optimized processes, BeSang is increasing density without compromising performance," he said.

BeSang's process works by first fabricating the logic on one wafer with normal vias and interconnection layers. Then memory devices are fabricated separately on a donor wafer, and the two wafers are aligned and bonded to form a single 3-D unit.

Because logic and memory are processed on different wafers, both can use normal 850-degree Celsius processes that have been separately optimized. The two wafers are then sent to another line, where they are precisely aligned and bonded using a proprietary low-temperature, 400-degree Celsius process.

The donor wafer essentially contains one vertically oriented bit cell, which, after bonding, is etched into millions of pillar-shaped transistors that control individual bit cells. The final step interconnects the individual bit cells and caps the 3-D wafer with final metallization layers.

"The cost of BeSang's 3-D chips should be much lower, because you are reducing the overall chip area by putting all your logic in one process on the bottom wafer, putting all of your memory, using a different process, on the top wafer, and using the conventional vias to interconnect them," Sze predicted.

Demonstration chips were processed on 8-inch wafers using 180-nanometer CMOS technologies. ■