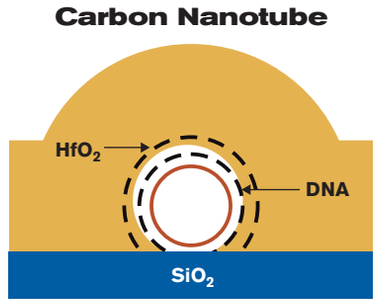
Open Facility for Nanofabrication

The Stanford Nanofabrication Facility (SNF)[1] is a state-of-the-art, shared-equipment laboratory open to academic, industrial and governmental researchers (Fig. 1). The 10,500 ft^2 cleanroom is located on the campus of Stanford University (Palo Alto, Calif.). Over 600 registered lab members research technologies ranging from MEMS, optics, biology and chemistry to traditional electronic device fabrication and process characterization. In this environment, personnel with expertise in process equipment assist in transforming ideas into working devices. Since opening in 1985, hundreds of projects have successfully passed through the SNF, leading to the realization of advanced devices, such as carbon nanotube (CNT) field-effect transistors (FETs), nanocavity array lasers and single-chip 3-D ICs.

1. Stanford Nanotechnology Facility is located in the Center for Integrated Systems on the Stanford University campus.

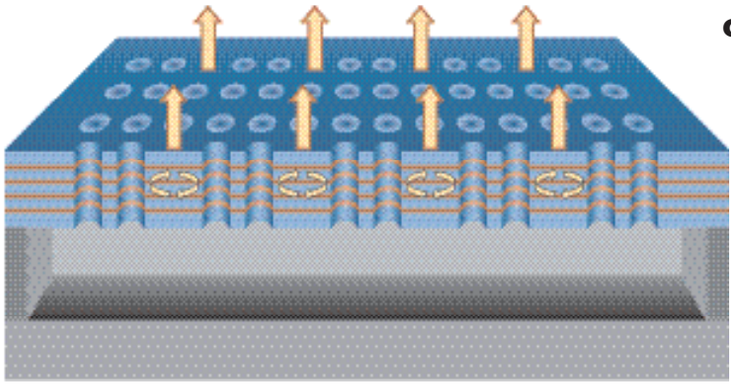
Carbon nanotube FETs

"A primary goal of transistor downscaling is to obtain low subthreshold swing approaching the theoretical limit of 60 mV/decade for device operations at low voltages and power dissipations," said Yuerui Lu, department of physics and Center for Integrated Systems at Stanford. One approach investigated is the application of single-walled carbon nanotubes (SWNTs) — advanced quasi-1-D materials — to making SWNT FETs. Because of the high-mobility of CNT FETs, near-ballistic electrical transport, chemical robustness, absence of surface dangling bonds, and sustained electrical properties are possible. However, to fabricate these devices requires thin, uniform gate insulator layers, which, until recently, have evaded researchers.

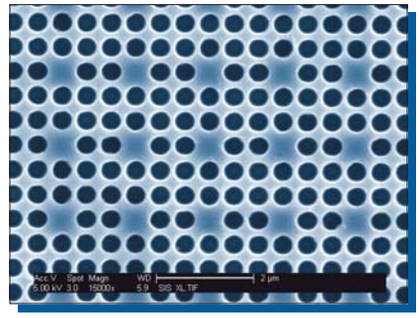


2. A cross-sectional view of the coating profiles of the nanotube (left).

A solution developed by Lu, in collaboration with Center members, Yoshio Nishi and Hongjie Dai, fabricates conformal uniform dielectric layers on CNT transistors[2] by first lining the outer surface of the CNT with poly-T-DNA molecules (Fig. 2). To avert the severe gate leakage and shorts observed in most of the SWNT FETs with high-k thicknesses and oxides <5 nm, the poly%-DNA is soaked in deionized (DI) water for 30 min followed by a 2 min sonication. Atomic layer deposition (ALD) is then used to deposit a thin (~2-3 nm) hafnium oxide gate insulator layer. The uniformity of the structure creates devices that can reliably achieve 60 mV/decade turn-on characteristics and a transconductance of 5000 siemens (g_m)/m, noted Lu. The researchers anticipate that reducing the high-k gate dielectric thicknesses from 10 to



Crystal Nanocavity Array Laser



3. The SEM (right) shows an InP-based photonic crystal cavity array laser. The schematic (left) illustrates the coupling of the nanocavities.

2-3 nm in device designs, such as a PIN structure, can lead to band-to-band tunneling transistors with turn-on characteristics beating the 60 mV/decade limit of conventional FETs.

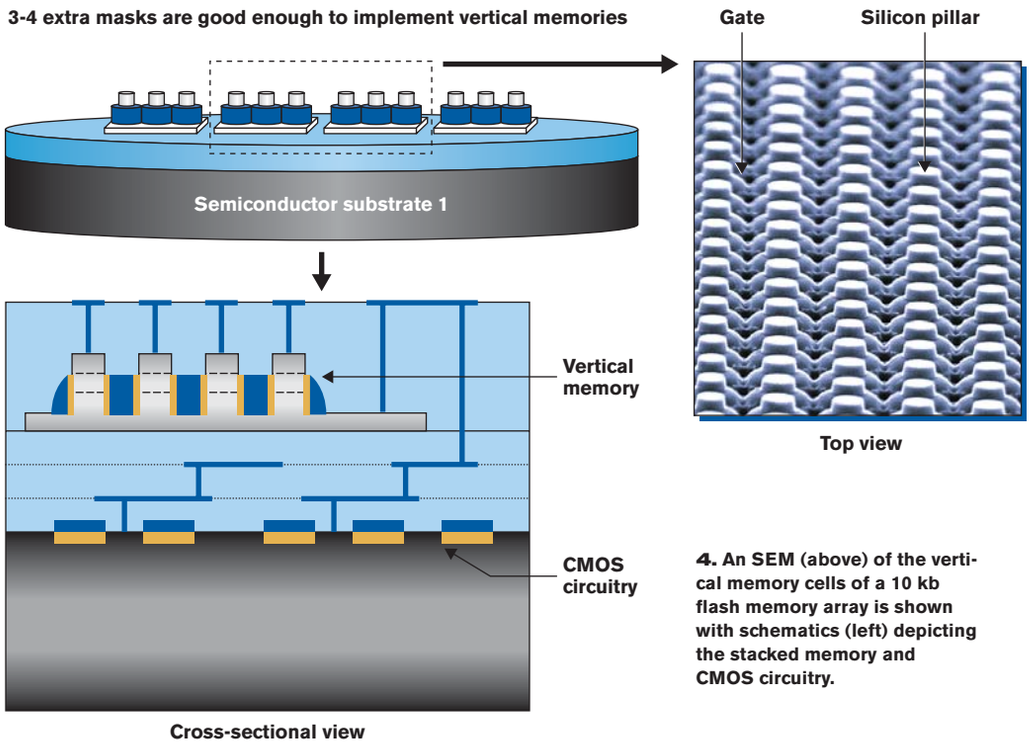
Nanocavity array lasers

Photonic crystal nanocavity array lasers were first demonstrated at the SNF. Developed as an alternative to vertical cavity surface emitting lasers (VCSEL), the arrays can achieve modulation speeds of 100 GHz-1 THz, 50-1000× faster than commercially available VCSELs, noted Jelena Vuckovic, professor at Stanford. To increase the modulation bandwidth in VCSELs, the photon density can be increased through stronger pumping; however, the heat generated leads to thermal instabilities. Moreover, with a larger emitting aperture, typically 10 µm in diameter, multimode operation, poor efficiencies and high thresholds are common in VCSELs. In principle, the array laser can resolve these limitations by placing as many as 100 photonic crystal lasers on a 10 µm square, thereby producing optical powers on the order of milliwatts (Fig. 3).

The nanocavity laser devices are fabricated using e-beam lithography, combined with dry and wet etching in an indium phosphide (InP)-based material system. The structure consists of a suspended (freestanding) InP membrane ~300 nm thick. The active region contains four indium gallium arsenide phosphide (InGaAsP) quantum wells embedded inside of the membrane, with a peak photoluminescence emission wavelength of 1560 nm. The membrane is patterned with an array of air holes. Each omitted hole inside of the array acts as a nanoresonator that localizes light. Periodic arrangement of these nanoresonators (spaced at 1.5 µm intervals) forms a nanocavity laser array. The strong localization of light in the photonic crystal lasers produces large photon densities and, thus, much higher modulation speeds than can be achieved in VCSELs.

The array of holes are defined in a poly methyl methacrylate resist layer using e-beam, and then transferred using a SiO_2 plasma etch mask. The oxide mask is used to etch the InGaAsP layer using a chlorine/argon/boron trichloride plasma etch. A sacrificial InP layer is then removed to suspend the active photonic crystal layer membrane. The hole spacing is 500 nm, and the radius ranges from 160 to 230 nm to change the resonance frequency of the cavities.

Vuckovic's group has demonstrated arrays of up to 3600 coupled photonic crystal nanocavity arrays in silicon and up to 81 cavities in InP- and GaAs-based materials. By ultradense coupling of nanocavity lasers, the differential quantum efficiencies were shown to be dramatically improved without sacrificing low lasing thresholds of single photonic crystal lasers. The high efficiency and low threshold are due to the large spontaneous emission coupling factors of the coupled nanolasers; that is, almost all of the emitted photons are channeled into the lasing mode in such lasers so pump power is not wasted on generating light outside the lasing mode.[3] Using a 2-D array of coupled nanocavities, the output of the laser was increased 100 times over a single photonic crystal cavity laser, comparable with single-mode VCSELs, but at lower-threshold pump powers. These promising structures are also capable of direct modulation at high speeds, approaching THz,[4] implying that coupled nanocavity arrays may be an effective way to achieve high-power and high-speed single-mode laser sources.



4. An SEM (above) of the vertical memory cells of a 10 kb flash memory array is shown with schematics (left) depicting the stacked memory and CMOS circuitry.

Single-chip 3-D technology

SNF research on 3-D ICs and multibit vertical flash memory technology led to the formation of the start-up company, BeSang Inc. (Portland, Ore.). "The single-chip 3-D process is designed to minimize

fabrication incompatibility issues," said Sangyun Lee, president and CEO. It is based on a surrounded gate transistor (SGT) structure, where the source, gate and drain are stacked. The vertical memory cells are then placed on top of a memory control logic wafer, effectively reducing the footprint and providing as much as 8× the effective cell density. When using the combination of a multibit stacked vertical SGT and a 3-D IC scheme, densities can reach 32× effective density, asserted Lee.

Processing begins with a conventional CMOS wafer that has been polished on top with chemical mechanical planarization (CMP) and a donor wafer containing predefined impurity layers for vertical memory cells (Fig. 4). The backside of the donor wafer is then removed, and a thin single crystalline silicon layer containing the predefined impurity layers is transferred to the top of the CMOS wafer. The silicon layer is ~3-6 µm thick if it is a photodiode or 0.5-1 µm if it is a memory device.

Conventional 3-D technology is traditionally used in packaging. Two CMOS wafers are typically bonded together, requiring large super-via landing pads at multiple points inside the chip to ensure proper alignment. Misalignment from wafer bonding could approach tens of microns. The greatest impact of this method is in the limited number of interconnections possible — a few hundred to a thousand.

BeSang's single-chip 3-D IC approach removes this limitation by bonding one CMOS wafer to an unpatterned doped donor wafer, requiring no wafer alignment. Electrical connections between the two layers are made using a standard photolithography process, producing a small margin for misalignment of <10 nm. Because the top memory layer is thin, typically <1.0 µm, super vias are not needed. Therefore, according to Lee, with the additional wafer real estate available, millions or billions of interconnections could be implemented as desired, potentially resulting in higher IC speeds.

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References

1. SNF is a member of the National Nanotechnology Infrastructure Network (NNIN), which is supported, in part, by the National Science Foundation under Grant ECS-9731293. For more information about SNF, go to: http://snf.stanford.edu.

2. Y. Lu et al., "DNA Functionalization of Carbon Nanotubes for Ultrathin Atomic Layer Deposition of High k Dielectrics for Nanotube Transistors with 60 mV/Decade Switching," *J. Am. Chem. Soc.*, 2006, Vol. 128, No. 11, p. 3518.

3. H. Altug and J. Vuckovic, "Photonic Crystal Nanocavity Array Laser," *Optics Express*, 2005, Vol. 13, No. 22, p. 8819.

4. D. Englund, H. Altug, I. Fushman and J. Vuckovic, "Terahertz Room-Temperature Photonic Crystal Nanocavity Laser," *Applied Physics Letters*, 2007, in press.

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