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COVER STORY

How 3D is Stacking Up

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Through-silicon vias (TSV) have captured the 3D packaging spotlight, as evidenced by crowded conference sessions, a tsunami of technical papers, and an increasing buzz about how great it's going to be — when they finally do it. Attracted by the growing demand for higher performance in less space, more than 50 companies are reportedly progressing towards commercializing TSV. The eventual winners must find paths that include acceptable prices, scalability, established supply chains, and

THE SHORT STORY

While moving towards tomorrow's high-performance 3D packages with through-silicon vias (TSV) has captured most of the attention in the industry, stacked packages and similar established approaches have many 3D advantages and are making substantial, if quieter, technical and market progress.

commercial payoffs large enough to justify their investments.

Meanwhile, in the shadow of this Tower of Babbling, 3D components continue to be produced in high volume by other methods. The producers are making quieter but steady progress to improve and extend the capabilities of proven 3D approaches, or even to introduce new, potentially disruptive ones.

The most recent 3D process, 3D silicon, was jointly announced on August 11th by **BeSang, Inc.**, South Korea's National Nanofab Center, and Stanford University Nanofab Center. This process creates a layer of active devices on a single silicon wafer, by stacking a processed silicon device layer from a donor wafer on top of the active device layer of a starting silicon wafer. The unique advantage of the process

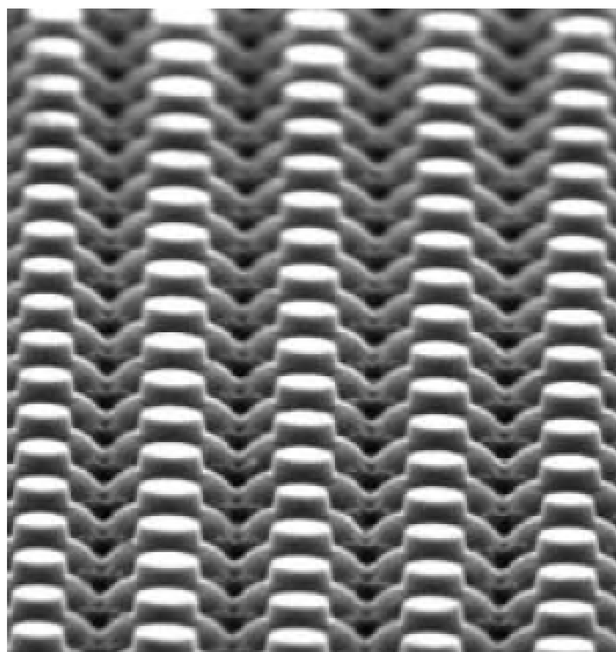

FIGURE 3. Portion of the 128M vertical transistor array, showing 0.8μm diameter pillars with surrounding gate conductor. *Courtesy of BeSang, Inc.*

is unrestricted 3D interconnection using conventional via technology, requiring neither wafer alignment nor TSVs.

For the demonstration units, the base wafer contains memory-control logic created with standard 180nm CMOS processes on 200mm wafers. Typical process temperatures are 850°C. The logic devices are finished with interconnection and via layers over the top surface.

The memory devices are created on a separate donor silicon wafer. It likewise is processed at 850°C to create the stacked doping layers required for vertical memory cells. The two wafers are bonded in a proprietary bonding process below 400°C, which transfers a single crystal doped silicon layer <1μm thick from the donor device to the base wafer. This transferred silicon layer is then patterned and metallized to create separate vertical transistor memory devices and connections.

The demonstration chips have 128M vertical transistors suitable for memory bit cells, positioned as a silicon layer with cells connected by simple vias to the control logic (Figure 3). In theory, the BeSang transfer process can be repeated to allow unlimited layer stacking. This creates high density stacking in the Z-axis, without resorting to increasingly painful shrinking in X and Y dimensions. The result could be significant cost and space savings.